CLAIMS

1. An architecture for a state machine (10) with a number of states of the machine, the architecture including a memory (14) having a set of addresses, wherein said memory is arranged to store at each of said addresses in the set the complete description of a respective one of said number of states of the machine (10).

2. The architecture of claim 1, characterised in that said memory (14) is clocked by a clock signal (CLK) and in that said memory (14) is arranged to switch from one state to another state within a single cycle of said clock signal (CLK).

3. The architecture of claim 1, characterised in that said memory (14) comprises at each address in said set a plurality of memory units adapted to be simultaneously selected to store a respective portion of said complete description of said respective one of said number of states of the machine (10).

4. The architecture of claim 3, characterised in that said plurality of memory units are mapped on an address plane with memory cells of a given length.

5. The architecture of claim 1, characterised in that said complete description of a respective one of said number of states of the machine (10) is partitioned in a number of sections, each said section describing a possible transition from said respective one state towards another state of said number of states of the machine (10).

6. The architecture of claim 1, characterised in that:

- said number of states of the machine (10) are expressed as binary values, and

- transitions between states of said number of states take place between a present state and a next state.

7. The architecture of claim 6, characterised in that the binary value for said next state is used to re-address said memory (14).

8. The architecture of claim 6, characterised in that it comprises a state register (16) to contain the binary value for said present state, said state register (16) being adapted to address said memory (14).

9. The architecture of claim 8, characterised in that it comprises a controller (18) to control access to said memory (14), said controller (18) being arranged to perform at least one of the functions selected from the group consisting of:

- causing said memory to be addressed via said state register (16),
- reset the contents of said state register (16),
- causing said state register to re-cycle through the same binary value.

10. The architecture of claim 1, characterised in that it comprises a controller (18) having a respective input line (EAB) to the state machine (10), said controller (18) being arranged to selectively feed said memory (14) with re-programming signals received over said respective input line.

11. The architecture of claim 10, characterised in that it comprises an output and state selector (12) having a set of input lines (IS) to the machine (10) and in that said respective input line (EAB) to said controller (18) is distinct from said input (IS) lines of said selector (12).

12. The architecture of claim 1, characterised in that it comprises an output and state selector (12) having a set of input lines (IS) to the machine (10) and in that said selector (12) comprises at least one line in said set of input lines (IS) adapted to receive input signals as two bit condition signals whereby said condition can be expressed as a three state signal (1,0,X).

13. The architecture of claim 6, characterised in that a default transition is provided among states of said number of states, said default transition including said next state as well as the values of said output signals (OS).

14. The architecture of claim 13, characterised in that said machine (10) is arranged to select said default transition when none of the conditions on the inputs of the other transitions is met.

15. The architecture of claim 13, characterised in that said machine (10) is a Moore machine and in that to each said transition there correspond the output values of said default transition.

16. The architecture of claim 6, characterised in that it comprises an output and state selector (12) having a set of input lines (IS) to the machine (10), said selector (12) including a plurality of comparators,

each of said comparators being adapted to receive over said set of input lines (IS) input signals as well as one of the possible input configurations described in the state description; said selector (12) being arranged to select a next state of said number of states as well as the corresponding set of output signals (OS) if one of said comparators provides a positive result, default values being selected in the absence of any such positive result.

17. The architecture of claim 1, characterised in that it comprises a plurality of counters for describing the state machine (10), said counters being provided as external components of said state machine (10), said counters being arranged to communicate with the said state machine (10) by means of at least one of an enable signal and an end-of-count signal.

18. The architecture of claim 1, characterised in that it comprises at least one computational block external with respect to said state machine (10), said at least computational block being arranged to communicate with said state machine (10) by means of at least one signal selected from the group consisting of the signals input to the machine (IS) and the signals output from the machine (OS).

19. The architecture of claim 17, characterised in that said counters have at least one of a reference value and an end-of-count value, said counters being arranged so that said at least one of said reference value and said end-of-count value can be modified run time.

20. The architecture of claim 17, characterised in that said counters comprise at least one re-writable

register adapted to contain a reference value for the respective counter.

21. The architecture of claim 1, characterised in that said memory (14) is a random access memory (RAM).

22. A method of executing a state machine (10) with a number of states of the machine, the method including the steps of:

- providing a memory (14) having a set of addresses, and
- storing at each of said addresses in the set the complete description of a respective one of said number of states of the machine (10).

23. The method of claim 22, characterised in that it comprises the steps of clocking said memory (14) by a clock signal (CLK) and switching said memory (14) from one state to another state within a single cycle of said clock signal (CLK).

24. The method of claim 22, characterised in that it comprises the steps of:

- providing at each address in said set a plurality of memory units,
- simultaneously selecting said plurality of memory units to store a respective portion of said complete description of said respective one of said number of states of the machine (10).

25. The method of claim 24, characterised in that it comprises the step of mapping said plurality of memory units on an address plane with memory cells of a given length.

26. The method of claim 22, characterised in that it comprises the step of partitioning said complete description of a respective one of said number of states of the machine (10) in a number of sections, each said section describing a possible transition from said respective one state towards another state of said number of states of the machine (10).

27. The method of claim 22, characterised in that it comprises the steps of :

- expressing said number of states of the machine (10) as binary values, and
- causing said transitions between states of said number of states to take place between a present state and a next state.

28. The method of claim 27, characterised in that it comprises the step of using the binary value for said next state to re-address said memory (14).

29. The method of claim 27, characterised in that it comprises the steps of providing a state register (16) containing the binary value for said present state, said state register (16) being adapted to address said memory (14).

30. The method of claim 29, characterised in that it comprises the step of controlling (18) access to said memory (14) by performing at least one of the functions selected from the group consisting of:

- causing said memory to be addressed via said state register (16),
- reset the contents of said state register (16),
- causing said state register to re-cycle through the same binary value.

31. The method of claim 22, characterised in that it comprises the steps of:

- providing a a respective input line (EAB) to the state machine (10), and
- selectively feeding said memory (14) with re-programming signals received over said respective input line.

32. The method of claim 31, characterised in that it comprises the step of providing output and state selector (12) having a set of input lines (IS) to the machine (10) and in that said respective input line (EAB) is distinct from said input (IS) lines of said selector (12).

33. The method of claim 22, characterised in that it comprises the step of providing a set of input lines (IS) to the machine (10) at least one line in said set of input lines (IS) being adapted to receive input signals as two bit condition signals whereby said condition can be expressed as a three state signal (1,0,X).

34. The method of claim 27, characterised in that a default transition is provided among states of said number of states, said default transition including said next state as well as the values of said output signals (OS).

35. The method of claim 34, characterised in that it comprises the step of arranging said machine (10) to select said default transition when none of the conditions on the inputs of the other transitions is met.

36. The method of claim 34, characterised in that said machine (10) is executedasd as a Moore machine by causing to each said transition to correspond the output values of said default transition.

37. The method of claim 27, characterised in that it comprises the steps of:

- providing a set of input lines (IS) to the machine (10) including a plurality of comparators,
- causing each of said comparators to receive input signals as well as one of the possible input configurations described in the state description;
- selecting a next state of said number of states as well as the corresponding set of output signals (OS) if one of said comparators provides a positive result, default values being selected in the absence of any such positive result.

38. The method of claim 22, characterised in that it comprises the step of providing a plurality of counters for describing the state machine (10), said counters being external components of said state machine (10) and arranged to communicate with the said state machine (10) by means of at least one of an enable signal and an end-of-count signal.

39. The method of claim 22, characterised in that it comprises the step of providing at least one computational block external with respect to said state machine (10) and arranged to communicate with said state machine (10) by means of at least one signal selected from the group consisting of the signals input to the machine (IS) and the signals output from the machine (OS).

40. The method of claim 38, characterised in that it comprises the steps of:
- providing said counters with at least one of a reference value and an end-of-count value, and
- modifying run time said at least one of said reference value and said end-of-count value.

41. The method of claim 38, characterised in that it comprises the step of providing at least one re-writable register for contain a reference value for the respective counter.

42. The method of claim 22, characterised in that said memory (14) is chosen as a random access memory (RAM).